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controller<and>bus<and>counter Search

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **An EPLD-based time-of-arrival acquisition board for neutron coincidence counting**
Fazzi, A.; Milano, D.; Varoli, V.;
Nuclear Science, IEEE Transactions on , Volume: 42 , Issue: 4 , Aug 1995
Pages:895 - 899

[Abstract] [PDF Full-Text (348 KB)] IEEE JNL

2 **Computers in the laboratory-an automatic data acquisition system**
Connelly, J.A.;
Frontiers in Education Conference, 1988., Proceedings , 22-25 Oct. 1988
Pages:24 - 30

[Abstract] [PDF Full-Text (424 KB)] IEEE CNF

3 **An integrated modeling system for dynamic operations control and real-time transit information**
Shalaby, A.; Farhan, A.;
Intelligent Transportation Systems, 2002. Proceedings. The IEEE 5th International Conference on , 2002
Pages:874 - 879

[Abstract] [PDF Full-Text (369 KB)] IEEE CNF

4 **Computer automated data acquisition and control for measurement of scintillati n materials and scintillating fibers**
Baumbaugh, B.W.; Bose, A.; Ditmire, T.; Kennedy, C.; Puseljic, D.; Ruchti, R.; Ryan, J.; Baumbaugh, A.; Knickerbocker, K.;
Nuclear Science, IEEE Transactions on , Volume: 37 , Issue: 2 , April 1990
Pages:298 - 304

[Abstract] [PDF Full-Text (576 KB)] IEEE JNL

5 **Optimal n nlinear transient c ntrol with neur -AVR f single-machine infinite-bus p wer systems**
Yazdanpanah, M.J.; Jalili-Kharaajoo, M.;
Decision and Control, 2003. Proceedings. 42nd IEEE Conference on , Volume: 2 , 9-12 Dec. 2003
Pages:1238 - 1243 Vol.2

[Abstract] [PDF Full-Text (426 KB)] IEEE CNF

6 **An EPLD-based time-of-arrival acquisition board for neutron coincidence counting**
Fazzi, A.; Milani, D.; Varoli, V.;
Nuclear Science Symposium and Medical Imaging Conference, 1994., 1994 IEEE Conference Record , Volume: 1 , 30 Oct.-5 Nov. 1994
Pages:346 - 350 vol.1

[Abstract] [PDF Full-Text (356 KB)] IEEE CNF

7 **A VXI based readout system for EUROGAM**
Aleonard, M.M.; Alexander, J.; Cresswell, J.; Gouillaud, J.C.; Karkour, N.; Lazarus, I.; McPherson, G.; Pedroza, J.L.; Pucknell, V.; Richard, A.; Ring, C.; Thornhill, J.; Wilkinson, L.;
Nuclear Science Symposium and Medical Imaging Conference, 1991., Conference Record of the 1991 IEEE , 2-9 Nov. 1991
Pages:868 - 872 vol.2

[Abstract] [PDF Full-Text (404 KB)] IEEE CNF

Terms used
c ntrollers and **bus** and **timeout** and **counter** and **network** and **error** and **alarm**

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1 Hardware fault containment in scalable shared-memory multiprocessors
Dan Teodosiu, Joel Baxter, Kinshuk Govil, John Chapin, Mendel Rosenblum, Mark Horowitz
May 1997 **ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture**, Volume 25 Issue 2
Full text available: pdf(2.05 MB) Additional Information: full citation, abstract, references, citings, index terms

Current shared-memory multiprocessors are inherently vulnerable to faults: any significant hardware or system software fault causes the entire system to fail. Unless provisions are made to limit the impact of faults, users will perceive a decrease in reliability when they entrust their applications to larger machines. This paper shows that fault containment techniques can be effectively applied to scalable shared-memory multiprocessors to reduce the reliability problems created by increased mach ...

2 Special session on reconfigurable computing: Adaptive architectures for an OTN processor: reducing design costs through reconfigurability and multiprocessing
Tudor Murgan, Mihail Petrov, Mateusz Majer, Peter Zipf, Manfred Glesner, Ulrich Heinkel, Joerg Pleickhardt, Bernd Bleisteiner
April 2004 **Proceedings of the first conference on computing frontiers on Computing frontiers**
Full text available: pdf(1.01 MB) Additional Information: full citation, abstract, references, citings, index terms

The standardisation process of Optical Transport Networks generally spans a long period of time. For providers intending to be present early on the market, this implies costly design re-spins if the wrong "flavour" of the protocol standard has been implemented. Extending a protocol processing device through application specific reconfigurable elements or multiprocessor units augment its flexibility. Thus, the architecture can be upgraded to standard updates or changes not even considered at desi ...

Keywords: ITU-T G.709, multiprocessor and reconfigurable architectures, optical transport networks, standard upgrades

3 Fast detection of communication patterns in distributed executions
Thomas Kunz, Michiel F. H. Seuren
November 1997 **Pr ceedings f the 1997 c nference f the Centre f r Advanced Studies n C llab rative research**

Full text available: pdf(4.21 MB) Additional Information: full citation, abstract, references, index terms

Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event tracer developed at the University of Waterloo. However, these diagrams are often very complex and do not provide the user with the desired overview of the application. In our experience, such tools display repeated occurrences of non-trivial commun ...

4 Xunet 2: lessons from an early wide-area ATM testbed

Charles R. Kalmanek, Srinivasan Keshav, William T. Marshall, Samuel P. Morgan, Robert C. Restrick

February 1997 **IEEE/ACM Transactions on Networking (TON)**, Volume 5 Issue 1

Full text available: pdf(231.69 KB) Additional Information: full citation, references, index terms

Keywords: asynchronous transfer mode, available bit rate, constant bit rate, variable bit rate

5 Multimicrocomputer system for building with full service facility automation

J. F. Tirado, J. J. Ruz, M. Mellado

August 1982 **Proceedings of the 5th ACM SIGSMALL symposium on Small systems**

Full text available: pdf(381.25 KB) Additional Information: full citation, abstract, references, index terms

The system here presented has been designed to be used on lodging establishments or institutions such as hotels, apartment buildings, hospitals, etc. The system picks up building generated data in order to provide the actual status of the building at any moment and performs status-dependent operations to provide: a) service to guest; b) security in the installment, and c) statistical and accounting information for management purposes. The aforementioned operations are realized by ...

6 Illustrative risks to the public in the use of computer systems and related technology

Peter G. Neumann

January 1996 **ACM SIGSOFT Software Engineering Notes**, Volume 21 Issue 1

Full text available: pdf(2.54 MB) Additional Information: full citation

7 Novanet communications network for a control system

J. R. Hill, J. R. Severyn, P. J. VanArsdall

October 1983 **ACM SIGCOMM Computer Communication Review , Proceedings of the eighth symposium on Data communications**, Volume 13 Issue 4

Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, references, index terms

Novanet is a control system oriented fiber optic local area network that was designed to meet the unique and often conflicting requirements of the Nova laser control system which will begin operation in 1984. The computers and data acquisition devices that form the distributed control system for a large laser fusion research facility need reliable, high speed communications. Both control/status messages and experimental data must be handled. A subset of NOVANET is currently operating on the ...

8 The space shuttle primary computer system

Alfred Spector, David Gifford

September 1984 **C mmunicati ns f the ACM**, Volume 27 Issue 9

Full text available: pdf(5.34 MB) Additional Information: full citation, references, citings, index terms

Keyw rds: PASS, avionics system, space shuttle

9 Twentenet: A LAN with message priorities, design and performance considerations.
I. G. Niemegeers, C. A. Vissers
June 1984 **ACM SIGCOMM Computer Communication Review , Proceedings of the ACM SIGCOMM symposium on Communications architectures and protocols: tutorials & symposium**, Volume 14 Issue 2
Full text available: pdf(731.45 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses design and performance aspects of Twentenet, one of the few implemented LANs which offers a service based on message priorities. The medium access mechanism uses the CSMA/CD principle, however with a deterministic collision resolution method. These characteristics make Twentenet suitable for real-time applications, as well as a mixture of real-time and non real-time applications. The general system structure is introduced followed by a detailed description of the priori ...

10 Performing remote operations efficiently on a local computer network
Alfred Z. Spector
April 1982 **Communications of the ACM**, Volume 25 Issue 4
Full text available: pdf(1.58 MB) Additional Information: full citation, abstract, references, citings, index terms

A communication model is described that can serve as a basis for a highly efficient communication subsystem for local networks. The model contains a taxonomy of communication instructions that can be implemented efficiently and can be a good basis for interprocessor communication. These communication instructions, called remote references, cause an operation to be performed by a remote process and, optionally, cause a value to be returned. This paper also presents implementation considerati ...

Keywords: communication models, efficient communication, transactions

11 Approximate performance analysis of real-time traffic over heavily loaded networks with timed token protocols
Jacek Świderski
June 1996 **IEEE/ACM Transactions on Networking (TON)**, Volume 4 Issue 3
Full text available: pdf(1.44 MB) Additional Information: full citation, references, index terms

12 A network combining packet switching and time division circuit switching in a common system
Joe de Smet, Ray W. Sanders
January 1976 **ACM SIGCOMM Computer Communication Review**, Volume 6 Issue 1
Full text available: pdf(1.25 MB) Additional Information: full citation

13 Searching for the sorting record: experiences in tuning NOW-Sort
Andrea C. Arpaci-Dusseau, Remzi H. Arpaci-Dusseau, David E. Culler, Joseph M. Hellerstein, David A. Patterson

August 1998 **Pr ceedings f the SIGMETRICS symp sium n Parallel and distributed t ls**
Full text available: pdf(1.37 MB) Additional Information: full citation, references, citings, index terms

14 Using channel state dependent packet scheduling to improve TCP throughput over wireless LANs
Pravin Bhagwat, Partha Bhattacharya, Arvind Krishma, Satish K. Tripathi
March 1997 **Wireless Networks**, Volume 3 Issue 1

Full text available: pdf(541.97 KB) Additional Information: full citation, abstract, references, citings, index terms

In recent years, a variety of mobile computers equipped with wireless communication devices have become popular. These computers use applications and protocols, originally developed for wired desktop hosts, to communicate over wireless channels. Unlike wired networks, packets transmitted on wireless channels are often subject to burst errors which cause back to back packet losses. In this paper we study the effect of burst packet errors and error recovery mechanisms employed in wireless MAC ...

15 Hypervisor-based fault tolerance
Thomas C. Bressoud, Fred B. Schneider
February 1996 **ACM Transactions on Computer Systems (TOCS)**, Volume 14 Issue 1

Full text available: pdf(1.89 MB) Additional Information: full citation, abstract, references, citings, index terms

Protocols to implement a fault-tolerant computing system are described. These protocols augment the hypervisor of a virtual-machine manager and coordinate a primary virtual machine with its backup. No modifications to the hardware, operating system, or application programs are required. A prototype system was constructed for HP's PA-RISC instruction-set architecture. Even though the prototype was not carefully tuned, it ran programs about a factor of 2 slower than a bare machine would.
Keywords: fault-tolerant computing system, primary/backup approach, virtual-machine manager

16 A parallel embedded-processor architecture for ATM reassembly
Richard F. Hobson, P. S. Wong
February 1999 **IEEE/ACM Transactions on Networking (TON)**, Volume 7 Issue 1

Full text available: pdf(331.21 KB) Additional Information: full citation, references, citings, index terms

Keywords: ATM, embedded systems, medium access control, segmentation and reassembly

17 AMp: a highly parallel atomic multicast protocol
P. Veríssimo, L. Rodrigues, M. Baptista
August 1989 **ACM SIGCOMM Computer Communication Review , Symposium pr ceedings n C mmunicati ns architectures & pr t c ls**, Volume 19 Issue 4

Full text available: pdf(1.40 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper deals with the problem of reliable group communication for distributed applications, in the context of the Reliable Broadcast class of protocols. An atomic multicast protocol for token passing Lans is presented. The actual implementation is on an 8802/4

Token-bus, although it is applicable to 8802/5 Token-rings and the FDDI Fibre-Optic network. The simplicity and efficiency of reliable broadcast protocols may be considerably improved, if the system fault model is restr ...

18 Remote queues: exposing message queues for optimization and atomicity

Eric A. Brewer, Frederic T. Chong, Lok T. Liu, Shamik D. Sharma, John D. Kubiatowicz

July 1995 **Proceedings of the seventh annual ACM symposium on Parallel algorithms and architectures**

Full text available: pdf(1.78 MB) Additional Information: full citation, references, citings, index terms

19 Recovery in the Calypso file system

Murthy Devarakonda, Bill Kish, Ajay Mohindra

August 1996 **ACM Transactions on Computer Systems (TOCS)**, Volume 14 Issue 3

Full text available: pdf(318.88 KB) Additional Information: full citation, abstract, references, citings, index terms, review

This article presents the deign and implementation of the recovery scheme in Calypso. Calypso is a cluster-optimized, distributed file system for UNIX clusters. As in Sprite and AFS, Calypso servers are stateful and scale well to a large number of clients. The recovery scheme in Calypso is nondisruptive, meaning that open files remain open, client modified data are saved, and in-flight operations are properly handled across server recover. The scheme uses distributed state amount the client ...

Keywords: Calypso, cluster systems, distributed state, state reconstruction

20 The information furnace: consolidated home control

Diomidis D. Spinellis

May 2003 **Personal and Ubiquitous Computing**, Volume 7 Issue 1

Full text available: pdf(488.36 KB) Additional Information: full citation, abstract, index terms

The Information Furnace is a basement-installed PC-type device that integrates existing consumer home-control, infotainment, security and communication technologies to transparently provide accessible and value-added services. A modern home contains a large number of sophisticated devices and technologies. Access to these devices is currently provided through a wide variety of disparate interfaces. As a result, end users face a bewildering array of confusing user-interfaces, access modes a ...

Keywords: Automation, Consumer electronics, Home-control, Multi-modal interfaces

Terms used
controllers and **bus** and **timeout** and **counter** and **network** and **error** and **alarm**

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21 New models and architectures: An ultra low-power processor for sensor networks

Virantha Ekanayake, Clinton Kelly, Rajit Manohar

October 2004 **Proceedings of the 11th international conference on Architectural support for programming languages and operating systems**

Full text available: pdf(437.23 KB) Additional Information: full citation, abstract, references, index terms

We present a novel processor architecture designed specifically for use in low-power wireless sensor-network nodes. Our sensor network asynchronous processor (SNAP/LE) is based on an asynchronous data-driven 16-bit RISC core with an extremely low-power idle state, and a wakeup response latency on the order of tens of nanoseconds. The processor instruction set is optimized for sensor-network applications, with support for event scheduling, pseudo-random number generation, bitfield operations, and ...

Keywords: asynchronous, event-driven, low-energy, picojoule computing, sensor network processor, sensor networks, wireless

22 The butterfly satellite IMP for the wideband packet satellite network

W Edmond, S Bumenthal, A Echenique, S Storch, T Calderwood

August 1986 **ACM SIGCOMM Computer Communication Review , Proceedings of the ACM SIGCOMM conference on Communications architectures & protocols**, Volume 16 Issue 3

Full text available: pdf(1.04 MB) Additional Information: full citation, abstract, references, citings, index terms

Multiprocessor computer systems have proven effective as high performance switching nodes in packet switched data communications networks. They are well suited to performing the required queuing, routing, and scheduling tasks, and can scale upward to provide higher system throughput when combined with software that exploits the parallelism provided by the hardware. This paper describes the packet switch used in the DARPA Wideband Packet Satellite Network and the Butterfly™ Multiproces ...

23 SODA: A simplified operating system for distributed applications

Jonathan Kepecs, Marvin Solomon

August 1984 **Pr ceedings f the third annual ACM symp sium n Principles f distributed c mputing**

Full text available: pdf(925.18 KB) Additional Information: full citation, abstract, references, citings, index terms

The design and implementation study discussed in this paper can be viewed in two ways. On one hand, it represents a contribution to the active area of design of "smart" communications controllers which use increasingly sophisticated processor/memory configurations to improve the performance of interprocessor communication. On the other hand, it represents an application of the minimalist principles of the RISC (Reduced Instruction-Set Computer) architecture [1] to operating syst ...

24 Performance analysis of several back-end database architectures

Robert Brian Hagmann, Domenico Ferrari

March 1986 **ACM Transactions on Database Systems (TODS)**, Volume 11 Issue 1

Full text available: pdf(1.54 MB) Additional Information: full citation, abstract, references, citings, index terms, review

The growing acceptance of database systems makes their performance increasingly more important. One way to gain performance is to off-load some of the functions of the database system to aback-end computer. The problem is what functions should be off-loaded to maximize the benefits of distributed processing. Our approach to this problem consisted of constructing several variants of an existing relational database system. INGRES, that partition the database system software into tw ...

25 SODA: a simplified operating system for distributed applications

Jonathan Kepecs, Marvin Solomon

October 1985 **ACM SIGOPS Operating Systems Review**, Volume 19 Issue 4

Full text available: pdf(1.05 MB) Additional Information: full citation, references, citings

26 Applications of model checking at Honeywell Laboratories

Darren Cofer, Eric Engstrom, Robert Goldman, David Musliner, Steve Vestal

May 2001 **Proceedings of the 8th international SPIN workshop on Model checking of software**

Full text available: pdf(93.14 KB) Additional Information: full citation, abstract, references

This paper provides a brief overview of five projects in which Honeywell has successfully used or developed model checking methods in the verification and synthesis of safety-critical systems.

27 Distributed operating systems

Andrew S. Tanenbaum, Robbert Van Renesse

December 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 4

Full text available: pdf(5.49 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Distributed operating systems have many aspects in common with centralized ones, but they also differ in certain ways. This paper is intended as an introduction to distributed operating systems, and especially to current university research about them. After a discussion of what constitutes a distributed operating system and how it is distinguished from a computer network, various key design issues are discussed. Then several examples of current research projects are examined in some detail ...

28 NTP retrospective: A brief history of NTP time: memoirs of an Internet timekeeper

David L. Mills

April 2003 **ACM SIGCOMM C mputer C mmunicati n Review**, Volume 33 Issue 2

Full text available: pdf(185.93 KB) Additional Information: full citation, abstract, references

This paper traces the origins and evolution of the Network Time Protocol (NTP) over two decades of continuous operation. The technology has been continuously improved from hundreds of milliseconds in the rowdy Internet of the early 1980s to tens of nanoseconds in the Internet of the new century. It includes a blend of history lessons, technology milestones and series of experiments that shape, define and record the early history of the Internet and NTP.This narrative is decidedly personal, since ...

Keywords: algorithmic memoirs, computer network, technical history, time synchronization

29 A dual processor VAX 11/780

George H. Goble, Michael H. Marsh

April 1982 **Proceedings of the 9th annual symposium on Computer Architecture**

Full text available: pdf(744.32 KB) Additional Information: full citation, abstract, references, index terms

This paper describes the design of a dual processor VAX 11/780 built at the Purdue University Electrical Engineering School. It covers the conversion of a standard single processor VAX 11/780 into a dual processor system. A detailed description of hardware modifications performed and a parts list are included. The dual processor VAX is currently running a modified version of the UNIX (Fourth Berkeley Distribution) operating system. Because of licensing restrictions, operating sys ...

30 Memory system performance of UNIX on CC-NUMA multiprocessors

John Chapin, A. Herrod, Mendel Rosenblum, Anoop Gupta

May 1995 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1995 ACM SIGMETRICS joint international conference on Measurement and modeling of computer systems**, Volume 23 Issue 1

Full text available: pdf(1.78 MB) Additional Information: full citation, abstract, references, citings, index terms

This study characterizes the performance of a variant of UNIX SVR4 on a large shared-memory multiprocessor and analyzes the effects of possible OS and architectural changes. We use a nonintrusive cache miss monitor to trace the execution of an OS-intensive multiprogrammed workload on the Stanford DASH, a 32-CPU CC-NUMA multiprocessor (CC-NUMA multiprocessors have cache-coherent shared memory that is physically distributed across the machine). We find that our version of UNIX accounts for 24% of ...

31 Analyzing communication latency using the Nectar communication processor

Peter Steenkiste

October 1992 **ACM SIGCOMM Computer Communication Review , Conference proceedings on Communications architectures & protocols**, Volume 22 Issue 4

Full text available: pdf(1.16 MB) Additional Information: full citation, abstract, references, citings, index terms

For multicomputer applications, the most important performance parameters of a network is the latency for short messages. In this paper we present an analysis of communication latency using measurement of the Nectar system. Nectar is a high-performance multicomputer built around a high-bandwidth crosspoint network. Nodes are connected to the Nectar network using network coprocessors that are primarily responsible the protocol processing, but that can also execute application code. This arch ...

32 Queue pair IP: a hybrid architecture for system area networks

Philip Buonadonna, David Culler

May 2002 **ACM SIGARCH C mputer Architecture News**, Volume 30 Issue 2

Full text available: pdf(1.01 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We propose a SAN architecture called Queue Pair IP (QPIP) that combines the interface from industry proposals for low overhead, high bandwidth networks, e.g. Infiniband, with the well established inter-network protocol suite. We evaluate how effectively the queue pair abstraction enables inter-network protocol offload. We develop a prototype QPIP system that implements basic queue pair operations over a subset of TCP, UDP and IPv6 protocols using a programmable network adapter. We assess this pr ...

Keywords: Interconnection Networks, Network Interfaces, Internetworking, Distributed Computing

33 The Parallel Protocol Engine

Matthias Kaiserswerth
December 1993 **IEEE/ACM Transactions on Networking (TON)**, Volume 1 Issue 6

Full text available: pdf(1.65 MB) Additional Information: full citation, references, citings, index terms, review

34 Preliminary thoughts on problem-oriented shared memory: a decentralized approach to distributed systems

David R. Cheriton
October 1985 **ACM SIGOPS Operating Systems Review**, Volume 19 Issue 4

Full text available: pdf(1.05 MB) Additional Information: full citation, abstract, references, citings

Much of the work to date on distributed systems has focused on the correct choice of *communication paradigm*, stressing (for example) message primitives, remote procedure call, problem- oriented protocols and so on. A distributed system service is then implemented as a module executing on particular server machine that is accessed using these communication facilities. In contrast, the shared *memory paradigm* has been used on multiprocessor and uniprocessor systems. In the shared memo ...

35 HIP: hybrid interrupt-polling for the network interface

Constantinos Dovrolis, Brad Thayer, Parameswaran Ramanathan
October 2001 **ACM SIGOPS Operating Systems Review**, Volume 35 Issue 4

Full text available: pdf(989.34 KB) Additional Information: full citation, abstract, references, index terms

The standard way to notify the processor of a network event, such as the arrival or transmission of a packet, is through interrupts. Interrupts are more effective than polling, in terms of the per packet send/receive latency. Interrupts, however, incur a high overhead both during and after the interrupt handling, because modern superscalar processors use long pipelines, out-of-order and speculative execution, and multi-level memory systems, all of which tend to increase the interrupt overhead in ...

36 Communication protocol design to facilitate re-use based on the object-oriented paradigm

Andrew A. Hanish, Tharam S. Dillon
December 1997 **M bile Netw rks and Applicati ns**, Volume 2 Issue 3

Full text available: pdf(609.13 KB) Additional Information: full citation, abstract, references, index terms

The main motivation for the present work stems from the wide gap which exists between the research efforts devoted to developing formal descriptions for communication protocols and the effective development methodologies used in industrial implementations. We apply Object-Oriented (OO) modelling principles to networking protocols, exploring the potential

for producing re-useable software modules by discovering the underlying generic class structures and behaviour. Petri Nets (PNs) are used ...

37 Distributed systems - programming and management: On remote procedure call

Patrícia Gomes Soares

November 1992 **Proceedings f the 1992 c nference f the Centre f r Advanced Studies on Collaborative research - Volume 2**

Full text available: pdf(4.52 MB) Additional Information: full citation, abstract, references, citings

The Remote Procedure Call (RPC) paradigm is reviewed. The concept is described, along with the backbone structure of the mechanisms that support it. An overview of works in supporting these mechanisms is discussed. Extensions to the paradigm that have been proposed to enlarge its suitability, are studied. The main contributions of this paper are a standard view and classification of RPC mechanisms according to different perspectives, and a snapshot of the paradigm in use today and of goals for t ...

38 On-line communications and the computer

F. K. Morioka, R. M. Wainwright

October 1969 **Proceedings of the first ACM symposium on Problems in the optimization of data communications systems**

Full text available: pdf(2.04 MB) Additional Information: full citation, abstract, index terms

This paper contains information on the general characteristics of the Control Data Corporation, MDM Communications Division M1000 Communications Message Switching System. It is the intent of this paper to discuss the analytic systems approach to the problem that led to the building of unique hardware and software to resolve the message handling functions. The M1000 hardware and software system features are discussed in the paper.

39 The minerva multi-microprocessor

Lawrence C. Widdoes

January 1976 **ACM SIGARCH Computer Architecture News , Proceedings of the 3rd annual symposium on Computer architecture**, Volume 4 Issue 4

Full text available: pdf(651.29 KB) Additional Information: full citation, abstract, references, citings, index terms

A multiprocessor system is described which is an experiment in low cost, extensible, multiprocessor architectures. Global issues such as inclusion of a central bus, design of the bus arbiter, and methods of interrupt handling are considered. The system initially includes two processor types, based on microprocessors, and these are discussed. Methods for reducing processor demand for the central bus are described.

40 Formal verification and analysis of multimedia systems

Sérgio Campos, Berthier Ribeiro-Neto, Autran Macedo, Luciano Bertini

October 1999 **Proceedings of the seventh ACM international conference on Multimedia (Part 1)**

Full text available: pdf(1.35 MB) Additional Information: full citation, abstract, references, index terms

Multimedia systems such as video-on-demand (VOD) servers are time critical systems. These systems have strict response times, which implies that a delayed response can have serious consequence. For instance, in the case of a VOD server, an immediate consequence of a delayed response time can be user dissatisfaction, what can ultimately lead to the end of a business based on this system. Therefore, analysis and verification of timing properties of multimedia systems is an important problem. ...

Terms used
c ntrollers and **bus** and **timeout** and **counter** and **network** and **error** and **alarm**

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41 Attack detection: Visualization of wormholes in sensor networks

Weichao Wang, Bharat Bhargava

October 2004 **Proceedings of the 2004 ACM workshop on Wireless security**

Full text available: pdf(919.82 KB) Additional Information: full citation, abstract, references, index terms

Several protocols have been proposed to defend against wormholes in ad hoc networks by adopting positioning devices, synchronized clocks, or directional antennas. In this paper, we propose a mechanism, MDS-VOW, to detect wormholes in a sensor network. MDS-VOW first reconstructs the layout of the sensors using multi-dimensional scaling. To compensate the distortions caused by distance measurement errors, a surface smoothing scheme is adopted. MDS-VOW then detects the wormhole by visualizing the a ...

Keywords: multi-dimensional scaling, sensor networks, visualization, wormhole attacks

42 Waiting algorithms for synchronization in large-scale multiprocessors

Beng-Hong Lim, Anant Agarwal

August 1993 **ACM Transactions on Computer Systems (TOCS)**, Volume 11 Issue 3

Full text available: pdf(2.72 MB) Additional Information: full citation, abstract, references, citings, index terms

Through analysis and experiments, this paper investigates two-phase waiting algorithms to minimize the cost of waiting for synchronization in large-scale multiprocessors. In a two-phase algorithm, a thread first waits by polling a synchronization variable. If the cost of polling reaches a limit Lpoll and further waiting is necessary, the thread is blocked, incurring an additional fixed cost, B. The choice of Lpoll

Keywords: barriers, blocking, competitive analysis, locks, producer-consumer synchronization, spinning, waiting time

43 The NSFNET backbone network

D. L. Mills, H. Braun

August 1987 **ACM SIGCOMM C mputer C mmunicati n Review , Pr ceedings f the ACM w rksh p n Fr ntiers in c mputer c mmunicati ns techn l gy,** Volume 17 Issue 5

Full text available: pdf(857.05 KB) Additional Information: full citation, abstract, references, citings, index terms

The NSFNET Backbone Network interconnects six supercomputer sites, several regional networks and ARPANET. It supports the DARPA Internet protocol suite and DCN subnet protocols, which provide delay-based routing and very accurate time-synchronization services. This paper describes the design and implementation of this network, with special emphasis on robustness issues and congestion-control mechanisms.

44 Replication in the harp file system

Barbara Liskov, Sanjay Ghemawat, Robert Gruber, Paul Johnson, Liuba Shrira

September 1991 **ACM SIGOPS Operating Systems Review , Proceedings of the thirteenth ACM symposium on Operating systems principles**, Volume 25 Issue 5

Full text available: pdf(1.60 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the design and implementation of the Harp file system. Harp is a replicated Unix file system accessible via the VFS interface. It provides highly available and reliable storage for files and guarantees that file operations are executed atomically in spite of concurrency and failures. It uses a novel variation of the primary copy replication technique that provides good performance because it allows us to trade disk accesses for network communication. Harp is intended to be u ...

45 Hardware support for concurrent programming in loosely coupled multiprocessors

H. K. Reghbati, V. C. Hamacher

April 1978 **Proceedings of the 5th annual symposium on Computer architecture**

Full text available: pdf(663.80 KB) Additional Information: full citation, abstract, references, citings, index terms

Various possible implementation schemes for concurrent programming concepts are surveyed. Based upon this examination, computer design features are proposed which assist in the efficient realization of concurrent programming concepts in a multiprocessor machine which is constructed from a number of self-contained processors, each with its own random access memory. It is indicated how the proposed architecture provides hardware support for creating and terminating parallel execution paths. T ...

46 A security architecture for fault-tolerant systems

Michael K. Reiter, Kenneth P. Birman, Robbert van Renesse

November 1994 **ACM Transactions on Computer Systems (TOCS)**, Volume 12 Issue 4

Full text available: pdf(2.50 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Process groups are a common abstraction for fault-tolerant computing in distributed systems. We present a security architecture that extends the process group into a security abstraction. Integral parts of this architecture are services that securely and fault tolerantly support cryptographic key distribution. Using replication only when necessary, and introducing novel replication techniques when it was necessary, we have constructed these services both to be easily defensible against atta ...

Keywords: key distribution, multicast, process groups

47 System-level exploration of association table implementations in telecom network applications

Ch. Ykman-Couvreur, J. Lambrecht, A. Van Der Togt, F. Catthoor, H. De Man

November 2002 **ACM Transacti ns n Embedded C mputing Systems (TECS)**, Volume 1 Issue 1

Full text available: pdf(375.20 KB) Additional Information: full citation, abstract, references, index terms

We present a new exploration and optimization method at the system level to select customized implementations for dynamic data sets, as encountered in telecom network, database, and multimedia applications. Our method fits in the context of embedded system synthesis for such applications, and enables to further raise the abstraction level of the initial specification, where dynamic data sets can be specified without low-level details. Our method is suited for hardware and software implementation ...

Keywords: System-level exploration, memory management

48 Balancing performance and flexibility with hardware support for network architectures
Ilija Hadžić, Jonathan M. Smith
November 2003 **ACM Transactions on Computer Systems (TOCS)**, Volume 21 Issue 4
Full text available: pdf(719.03 KB) Additional Information: full citation, abstract, references, index terms

The goals of performance and flexibility are often at odds in the design of network systems. The tension is common enough to justify an architectural solution, rather than a set of context-specific solutions. The Programmable Protocol Processing Pipeline (P4) design uses programmable hardware to selectively accelerate protocol processing functions. A set of field-programmable gate arrays (FPGAs) and an associated library of network processing modules implemented in hardware are augmented with so ...

Keywords: FPGA, P4, computer networking, flexibility, hardware, performance, programmable logic devices, programmable networks, protocol processing

49 Architectural considerations for a microprogrammable emulating engine using bit-slices
C. Halatsis, A. van Dam, J. Joosten, M. Letheren
May 1980 **Proceedings of the 7th annual symposium on Computer Architecture**
Full text available: pdf(951.32 KB) Additional Information: full citation, abstract, references, index terms

This paper describes architectural considerations which led to the design of a fast programmable processor made from ECL bit-slioes. The processor will be used as an on-line data filtering engine for high energy physics experiments. Unlike prior designs of such engines, the processor supports both user (horizontal) microcode and emulation of the PDP-11 fixed point instruction set (without memory management and multiple interrupt levels). In addition to an overview of the techniques used to ...

50 Architecture of the space shuttle primary avionics software system
Gene D. Carlow
September 1984 **Communications of the ACM**, Volume 27 Issue 9
Full text available: pdf(1.26 MB) Additional Information: full citation, abstract, citings, index terms

PASS, perhaps the most complex flight computer program ever developed, epitomizes the benefits to be gained by establishing a well-structured system architecture at the front end of the development process

Keywords: PASS, PASS space shuttle, avionics system, space shuttle

51 Storage protocol designs: A study of iSCSI extensions for RDMA (iSER)
Mallikarjun Chadalapaka, Hemal Shah, Uri Elzur, Patricia Thaler, Michael Ko
August 2003 **Pr ceedings f the ACM SIGCOMM w rksh p n Netw rk-I/O c nvergence: experience, less ns, implicati ns**
Full text available: pdf(281.32 KB) Additional Information: full citation, abstract, references, index terms

The iSCSI protocol is the IETF standard that maps the SCSI family of application protocols onto TCP/IP enabling convergence of storage traffic on to standard TCP/IP fabrics. The ability to efficiently transfer and place the data on TCP/IP networks is crucial for this convergence of the storage traffic. The iWARP protocol suite provides Remote Direct Memory Access (RDMA) semantics over TCP/IP networks and enables efficient memory-to-memory data transfers over an IP fabric. This paper studies the ...

Keywords: DA, DDP, DI, Datamover, MPA, RDMA, RDMAP, SCSI, Verbs, iSCSI, iSER, iWARP

52 An SBus monitor board

H. A. Xie, K. E. Forward, K. M. Adams, D. Leask

February 1995 **Proceedings of the 1995 ACM third international symposium on Field-programmable gate arrays**

Full text available: pdf(68.64 KB) Additional Information: full citation, abstract, references, index terms

During the development of computer peripherals which interface to the processor via the system bus it is often necessary to acquire the signals on the bus at the hardware level. It is difficult to attach general-purpose logic analysers and in-circuit emulators to a multiple pin bus connector and hence it is not practical to catch all the bus data required to ensure that such signals are in accordance with the bus specification. Hence a given connector specific bus monitor board is a necessa ...

53 High-speed local area networks and their performance: a survey

Bandula W. Abeysundara, Ahmed E. Kamal

June 1991 **ACM Computing Surveys (CSUR)**, Volume 23 Issue 2

Full text available: pdf(3.83 MB) Additional Information: full citation, abstract, references, citings, index terms, review

At high data transmission rates, the packet transmission time of a local area network (LAN) could become comparable to or less than the medium propagation delay. The performance of many LAN schemes degrades rapidly when the packet transmission time becomes small comparative to the medium propagation delay. This paper introduces LANs and discusses the performance degradation of LANs at high speeds. It surveys recently proposed LAN schemes designed to operate at high data rates, including the ...

Keywords: access schemes, computer networks, data communication, medium access protocols, optical fiber networks

54 Havana: supporting application and channel dependent QoS in wireless packet networks

Javier Gomez, Andrew T. Campbell

January 2003 **Wireless Networks**, Volume 9 Issue 1

Full text available: pdf(325.55 KB) Additional Information: full citation, abstract, references, index terms

For wireless channels, interference mitigation techniques are typically applied at the packet transmission level. In this paper, we present the Havana framework which supports *integrated adaptive-QoS* in wireless packet networks by responding to impairments over multiple time scales that are present at the flow/session level. The Havana framework is based on three different control mechanisms that operate over distinct adaptation time scales. At the packet transmission time scale, a packet ...

Keyw rds: QoS, adaptive wireless networks

55 Analysis of concentrated ALOHA satellite links

Mart L. Molle, Leonard Kleinrock

November 1979 **Proceedings of the sixth symposium on Data communications**

Full text available: pdf(737.06 KB) Additional Information: full citation, abstract, references, index terms

A conventional ALOHA satellite link uses a transponder which blindly echoes all up-channel traffic on the down-channel. An ALOHA channel can never be fully utilized, so an intelligent satellite could statistically multiplex the successful packets from several slotted ALOHA up-channels onto a single down-channel to conserve bandwidth, and hence reduce cost. We refer to this as a concentrated ALOHA system. Throughput, delay and stability effects are considered, varying the number of up ...

56 Local networks

William Stallings

March 1984 **ACM Computing Surveys (CSUR)**, Volume 16 Issue 1

Full text available: pdf(3.01 MB) Additional Information: full citation, abstract, references, citings, index terms, review

The rapidly evolving field of local network technology has produced a steady stream of local network products in recent years. The IEEE 802 standards that are now taking shape, because of their complexity, do little to narrow the range of alternative technical approaches and at the same time encourage more vendors into the field. The purpose of this paper is to present a systematic, organized overview of the alternative architectures for and design approaches to local networks.

...

57 Wireless home networks: Design and implementation of the HiperLan/2 protocol

E. P. Vasilakopoulou, G. E. Karastergios, G. D. Papadopoulos

April 2003 **ACM SIGMOBILE Mobile Computing and Communications Review**, Volume 7 Issue 2

Full text available: pdf(1.50 MB) Additional Information: full citation, abstract, references

In recent years, wireless communication systems have experienced an enormous development, leading to the emergence of various wireless networks standards. These standards are characterized by different properties, such as their coverage, data rates, mobility and QoS support. Among them the HiperLan/2 standard is distinguished of its performance, supporting the provision of high-speed integrated services. Its centralized Medium Access Control protocol though is the most critical and complex funct ...

58 Columns: Risks to the public in computers and related systems

Peter G. Neumann

March 2001 **ACM SIGSOFT Software Engineering Notes**, Volume 26 Issue 2

Full text available: pdf(832.74 KB) Additional Information: full citation

59 Special session: Design and programming of embedded multiprocessors: an interface-centric approach

Pieter van der Wolf, Erwin de Kock, Tomas Henriksson, Wido Kruijtzer, Gerben Essink

September 2004 **Proceedings of the 2nd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

Full text available: pdf(377.96 KB) Additional Information: full citation, abstract, references, index terms

We present design technology for the structured design and programming of embedded multi-processor systems. It comprises a task-level interface that can be used both for

developing parallel application models and as a platform interface for implementing applications on multi-processor architectures. Associated mapping technology supports refinement of application models towards implementation. By linking application development and implementation aspects, the technology integrates the specificat ...

Keyw rds: code transformation, media processing, multiprocessor mapping, platform interface, system design method, task-level interface

60 Modeling methodology b: Simulation and verification II: event-triggered environments for verification of real-time systems

Darren D. Cofer, Murali Rangarajan

December 2003 **Proceedings of the 35th conference on Winter simulation: driving innovation**

Full text available: pdf(395.81 KB) Additional Information: full citation, abstract, references

The growing complexity and the safety-critical requirements of the embedded software in avionics systems present many challenges to current test-based verification technology. The use of formal verification methods can increase design assurance by exploring a larger range of system behaviors and fault conditions than can feasibly be covered by testing or simulation. However, one of the most challenging tasks faced in any formal verification activity is the construction of an adequate model fo ...

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Refine Search controllers and bus and timeout and counter and netwo

	PAT. NO.	Title
1	6,813,777	Transaction dispatcher for a passenger entertainment system, method and article of manufacture
2	6,731,625	System, method and article of manufacture for a call back architecture in a hybrid network with support for internet telephony
3	6,711,693	Method for synchronizing plurality of time of year clocks in partitioned plurality of processors where each partition having a microprocessor configured as a multiprocessor backplane manager
4	6,701,338	Cumulative status of arithmetic operations
5	6,681,282	Online control of a multiprocessor computer system
6	6,671,818	Problem isolation through translating and filtering events into a standard object format in a network based supply chain
7	6,658,540	Method for transaction command ordering in a remote data replication system
8	6,625,689	Multiple consumer-multiple producer rings
9	6,606,744	Providing collaborative installation management in a network-based supply chain environment
10	6,600,971	Distributed control network for irrigation management
11	6,421,730	Programmable system for processing a partitioned network infrastructure
12	6,401,117	Platform permitting execution of multiple network infrastructure applications
13	6,240,478	Apparatus and method for addressing electronic modules
14	6,157,955	Packet processing system including a policy engine having a classification unit
15	6,081,812	Identifying at-risk components in systems with redundant components
16	5,999,525	Method for video telephony over a hybrid network
17	5,940,771	Network supporting roaming, sleeping terminals
18	5,790,895	Modem sharing
19	5,790,546	Method of transmitting data packets in a packet switched communications network
20	5,687,388	Scalable tree structured high speed input/output subsystem architecture

21 5,642,350 Peer to peer network for a mobile radio transceiver
22 5,596,631 Station controller for distributed single line PABX
23 5,590,292 Scalable tree structured high speed input/output subsystem architecture
24 5,553,095 Method and apparatus for exchanging different classes of data during different time intervals
25 5,537,549 Communication network with time coordinated station activity by time slot and periodic interval number
26 5,521,910 Method for determining a best path between two nodes
27 5,493,571 Apparatus and method for digital communications with improved delimiter detection
28 5,491,694 System and method for allocating a shared resource among competing devices
29 5,491,531 Media access controller with a shared class message delivery capability
30 5,485,455 Network having secure fast packet switching and guaranteed quality of service
31 5,446,868 Network bridge method and apparatus
32 5,400,331 Communication network interface with screeners for incoming messages
33 4,964,120 Method of detecting a cable fault and switching to a redundant cable in a universal local area network
34 4,777,591 Microprocessor with integrated CPU, RAM, timer, and bus arbiter for data communications systems
35 4,646,232 Microprocessor with integrated CPU, RAM, timer, bus arbiter data for communication system
36 4,641,308 Method of internal self-test of microprocessor using microcode
37 4,571,675 Microprocessor device with integrated auto-loaded timer
38 4,521,871 Programmable controller with back-up capability
39 4,363,093 Processor intercommunication system

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((((((controllers AND bus) AND timeout) AND counter) AND network) AND error) AND alarm): 173 patents.
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Refine Search controllers and bus and timeout and counter and netwo

	PAT. NO.	Title
1	6,731,625	System, method and article of manufacture for a call back architecture in a hybrid network with support for internet telephony
2	6,724,757	Configurable network router
3	6,718,535	System, method and article of manufacture for an activity framework design in an e-commerce based environment
4	6,704,873	Secure gateway interconnection in an e-commerce based environment
5	6,687,339	Controller for use with communications systems for converting a voice message to a text message
6	6,671,818	Problem isolation through translating and filtering events into a standard object format in a network based supply chain
7	6,633,878	Initializing an ecommerce database framework
8	6,631,134	Method for allocating bandwidth in an optical network
9	6,609,128	Codes table framework design in an E-commerce architecture
10	6,606,744	Providing collaborative installation management in a network-based supply chain environment
11	6,601,233	Business components framework
12	6,600,971	Distributed control network for irrigation management
13	6,584,571	System and method of computer operating mode clock control for power consumption reduction
14	6,574,333	State machine based universal voice grade cards
15	6,563,821	Channel bonding in a remote communications server system
16	6,523,027	Interfacing servers in a Java based e-commerce architecture
17	6,421,754	System management mode circuits, systems and methods
18	6,377,543	Path restoration of networks

19 6,374,286 Real time processor capable of concurrently running multiple independent JAVA machines
20 6,366,217 Wide area remote telemetry
21 6,359,894 Remote communications server system
22 6,333,940 Integrated digital loop carrier system with virtual tributary mapper circuit
23 6,314,460 Method and apparatus for analyzing a storage network based on incomplete information from multiple respective controllers
24 6,289,375 Method and apparatus for invoking network agent functions using a hash table
25 6,253,240 Method for producing a coherent view of storage network by a storage network manager using data storage device configuration obtained from data storage devices
26 6,240,335 Distributed control system architecture and method for a material transport system
27 6,233,242 Network switch with shared memory system
28 6,222,840 Method and system for performing concurrent read and write cycles in network switch
29 6,201,789 Network switch with dynamic backpressure per port
30 6,157,464 Facsimile store and forward system with local interface
31 6,124,806 Wide area remote telemetry
32 6,112,273 Method and apparatus for handling system management interrupts (SMI) as well as, ordinary interrupts of peripherals such as PCMCIA cards
33 6,094,434 Network switch with separate cut-through buffer
34 6,091,737 Remote communications server system
35 6,081,752 Computer system having power supply primary sense to facilitate performance of tasks at power off
36 6,079,025 System and method of computer operating mode control for power consumption reduction
37 6,078,593 Method and apparatus for reliable operation of universal voice grade cards
38 6,061,809 Process control interface system having triply redundant remote field units
39 6,055,145 Overcurrent protection device with visual indicators for trip and programming functions
40 6,049,550 Integrated digital loop carrier system with virtual tributary mapper circuit
41 6,014,587 Electro-convulsive therapy (ECT) system with enhanced safety features
42 5,999,525 Method for video telephony over a hybrid network
43 5,987,244 Power management masked clock circuitry, systems and methods
44 5,970,226 Method of non-intrusive testing for a process control interface system having triply redundant remote field units
45 5,949,994 Dedicated context-cycling computer with timed context
46 5,943,507 Interrupt routing circuits, systems and methods
47 5,892,959 Computer activity monitor providing idle thread and other event sensitive clock and power control
48 5,875,312 Structure and method of performing DMA transfers between memory and I/O devices utilizing a single DMA controller within a notebook and docking station computer system
49 5,872,983 Power management interface system for use with an electronic wiring board article of manufacture
50 5,870,621 Quadrilateral multichip computer systems and printed circuit boards therefor

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Refine Search controllers and bus and timeout and counter and netwo

	PAT. NO.	Title
51	5,870,617	Systems, circuits and methods for mixed voltages and programmable voltage rails on integrated circuits
52	5,867,717	Dynamic system clocking and address decode circuits, methods and systems
53	5,864,702	Computer system power management interconnection circuitry, systems and methods
54	5,862,338	Polling system that determines the status of network ports and that stores values indicative thereof
55	5,862,315	Process control interface system having triply redundant remote field units
56	5,852,370	Integrated circuits for low power dissipation in signaling between different-voltage on chip regions
57	5,848,253	Computer system and an electronic circuit utilizing a single DMA controller and additional communication circuit to manage DMA transfers between memory and I/O devices
58	5,845,132	Computer system power management interconnection circuitry, system and methods
59	5,844,795	Diagnostic aid for industrial controller using multi-tasking architecture
60	5,842,005	Clock control circuits, systems and methods
61	5,835,733	Method and apparatus for implementing a single DMA controller to perform DMA operations for devices on multiple buses in docking stations, notebook and desktop computer system
62	5,831,851	Apparatus and method for controlling high throughput sputtering
63	5,822,550	Split data path fast at-bus on chip circuits systems and methods
64	5,805,854	System and process for memory column address organization in a computer system
65	5,802,555	Computer system including a refresh controller circuit having a row address strobe multiplexer and associated method
66	5,799,198	Activity monitor for computer system power management

67 5,784,377 Integrated digital loop carrier system with virtual tributary mapper circuit
68 5,784,291 CPU, memory controller, bus bridge integrated circuits, layout structures, system and methods
69 5,781,780 Power management supply interface circuitry, systems and methods
70 5,778,425 Electronic system having a first level write through cache memory and smaller second-level write-back cache memory and method of operating the same
71 5,771,373 Power management masked clock circuitry, systems and methods
72 5,760,704 Patient tracking system for hospital emergency facility
73 5,758,175 Multi-mode power switching for computer systems
74 5,758,174 Computer system having a plurality of stored system capability states from which to resume
75 5,755,744 Electro-convulsive therapy (ECT) system with enhanced safety features
76 5,754,837 Clock control circuits, systems and methods
77 5,754,436 Adaptive power management processes, circuits and systems
78 5,752,044 Computer system having multi-level suspend timers to suspend from operation in attended and unattended modes
79 5,737,765 Electronic system with circuitry for selectively enabling access to configuration registers used by a memory controller
80 5,737,764 Generation of memory column addresses using memory array type bits in a control register of a computer system
81 5,737,748 Microprocessor unit having a first level write-through cache memory and a smaller second-level write-back cache memory
82 5,737,563 Determination of memory bank sizes in a computer system
83 5,734,919 Systems, circuits and methods for mixed voltages and programmable voltage rails on integrated circuits
84 5,729,720 Power management masked clock circuitry, systems and methods
85 5,727,221 Computer system power management interconnection circuitry and systems
86 5,724,553 Electronic system with circuitry for generating memory column addresses using memory array type bits in a control register
87 5,721,933 Power management supply interface circuitry, systems and methods
88 5,715,464 Computer system having suspend once resume many sessions
89 5,713,006 Electronic device and method for selective enabling of access to configuration registers used by a memory controller
90 5,710,929 Multi-state power management for computer systems
91 5,710,911 Clock control circuits, systems and methods
92 5,689,715 Low power ring detect for computer system wake-up
93 5,684,997 Integrated circuit design for handling of system management interrupts (SMI)
94 5,640,002 Portable RF ID tag and barcode reader
95 5,630,142 Multifunction power switch and feedback led for suspend systems
96 5,627,716 Overcurrent protection device
97 5,621,731 Private exchange for ISDN
98 5,608,720 Control system and operations system interface for a network element in an access system
99 5,608,643 System for managing multiple dispensing units and method of operation
100 5,603,038 Automatic restoration of user options after power loss

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Refine Search controllers and bus and timeout and counter and netwo

	PAT. NO.	Title
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67 5,784,377 Integrated digital loop carrier system with virtual tributary mapper circuit
68 5,784,291 CPU, memory controller, bus bridge integrated circuits, layout structures, system and methods
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100 5,603,038 Automatic restoration of user options after power loss

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	PAT. NO.	Title
101	5,598,455	Alarm and test system for a digital added main line
102	5,581,692	Automatic clearing of power supply fault condition in suspend system
103	5,560,023	Automatic backup system for advanced power management
104	5,559,611	Facsimile store and forward system with local interface
105	5,555,100	Facsimile store and forward system with local interface translating DTMF signals into store and forward system commands
106	5,551,043	Standby checkpoint to prevent data loss
107	5,530,879	Computer system having power management processor for switching power supply from one state to another responsive to a closure of a switch, a detected ring or an expiration of a timer
108	5,519,618	Airport surface safety logic
109	5,511,204	Performing system tasks at power-off using system management interrupt
110	5,490,134	Versatile communications controller
111	5,477,858	Ultrasound blood flow/tissue imaging system
112	5,448,442	Motor controller with instantaneous trip protection
113	5,428,813	Special function micro controller integrated circuit programmed to selectively perform one of at least two different and unrelated functions
114	5,428,769	Process control interface system having triply redundant remote field units
115	5,404,401	Alarm and test system for a digital added main line
116	5,396,635	Power conservation apparatus having multiple power reduction levels dependent upon the activity of the computer system

117 5,386,183 Method and apparatus for sensing a ground fault in a motor control system
118 5,374,932 Airport surface surveillance system
119 5,270,898 Sure chip plus
120 5,255,086 Method and apparatus for RF data transfer in a CATV system
121 5,235,619 Cable television radio frequency subscriber data transmission apparatus and RF return method
122 5,225,902 Automatic frequency selection in a bi-directional cable television system
123 5,214,692 Bypass for telephone switching system
124 5,206,572 Motor controller
125 5,206,455 Laser initiated ordnance systems
126 5,195,125 Gel filled RJ11 connector
127 5,185,736 Synchronous optical transmission system
128 5,155,590 System for data channel level control
129 5,142,690 Cable television radio frequency data processor
130 5,134,691 Bidirectional communication and control network with programmable microcontroller interfacing digital ICs transmitting in serial format to controlled product
131 5,113,523 High performance computer system
132 5,111,497 Alarm and test system for a digital added main line
133 5,109,384 Guaranteed reliable broadcast network
134 5,045,816 Binary phase shift key modulator with programmable level control
135 5,036,518 Guaranteed reliable broadcast network
136 5,007,013 Bidirectional communication and control network with programmable microcontroller interfacing digital ICS and controlled product
137 4,972,452 Digital bypass for telephone system
138 4,972,368 Intelligent serial I/O subsystem
139 4,939,437 Motor controller
140 4,831,582 Database access machine for factory automation network
141 4,829,445 Distributed routing unit for fully-automated flexible manufacturing system
142 4,804,938 Distribution energy management system
143 4,777,633 Base station for wireless digital telephone system
144 4,625,081 Automated telephone voice service system
145 4,575,847 Hot carrier detection
146 4,570,217 Man machine interface
147 4,555,781 Conversational video system having local network control
148 4,555,595 Sampled port data switching system employing interactive processors
149 4,525,779 Conversational video system
150 4,491,946 Multi-station token pass communication system

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Refine Search controllers and bus and timeout and counter and netwo

	PAT. NO.	Title
151	4,479,034	Arrangement of interactive processors for control of ports
152	4,475,011	Arrangement of interactive telephone switching processors providing selective functional capability by port
153	4,471,169	Arrangement of interactive telephone switching processors and associated port data storage means
154	4,451,702	Arrangement of interactive telephone switching processors for performing timing analyses of port events
155	4,447,673	Ring trip apparatus for a line circuit connected to DCO switch
156	4,445,180	Plant unit master control for fossil fired boiler implemented with a digital computer
157	4,443,663	Filtering of port data in a switching system employing interactive processors
158	4,366,350	Control system for telephone switching system
159	4,325,120	Data processing system
160	4,314,334	Serial data communication system having simplex/duplex interface
161	4,306,803	Microprocessor and control apparatus in a photocopier
162	4,300,230	Digital switching arrangements for stored program control telecommunications systems
163	4,283,773	Programmable master controller communicating with plural controllers
164	4,280,060	Dedicated micŕocomputer-based control system for steam turbine-generators
165	4,276,451	Control system for telephone switching system
166	4,271,505	Process communication link
167	4,253,146	Module for coupling computer-processors
168	4,245,306	Selection of addressed processor in a multi-processor network
169	4,190,350	Distributed microprocessor control system for a copier/duplicator

170 4,183,089 Data communications system for a reproduction machine having a master and secondary controllers
171 4,170,791 Serial data communication system for a reproduction machine
172 4,144,550 Reproduction machine using fiber optics communication system
173 4,030,072 Computer system operation and control

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